AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A static flip-flop circuit ~~characterized in that it~~ comprises~~ing~~:

a master circuit ~~including~~comprising a first data reading differential pair, a first data-hold differential pair ~~composed of~~comprising transistors of a size smaller than ~~the~~ transistors ~~constituting~~comprising the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair; and

a slave circuit ~~including~~comprising a second data reading differential pair, a second data-hold differential pair ~~composed~~comprising ~~of~~transistors of a size smaller than ~~the~~ transistors ~~constituting~~comprising the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair~~;~~;

wherein the flip-flop circuit operates in an operating speed range in which the currents through the first and second data-hold differential pairs are lower than the currents through the first and second data reading differential pairs, and the currents through the first and second data-hold differential pairs are equal to or lower than the permissible current level of the transistors that constitute the data-hold differential pairs.

2. (withdrawn) A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of transistors of a size smaller than the transistors constituting the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair;

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of transistors of a size smaller than the transistors constituting the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair; and

a current control terminal connected to the first and second current source circuits for controlling the currents through the first and second data reading differential pairs and the currents through the first and second data-hold differential pairs, in accordance with the operating speed of the flip-flop circuit.

3. (withdrawn): The static flip-flop circuit according to Claim 2, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the current control terminal adjusts the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

4. (withdrawn): A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of transistors of a size smaller than the transistors constituting the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair;

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of transistors of a size smaller than the transistors constituting the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair;

a first integrating circuit interposed between the first current source circuit for the master circuit and the terminal to which a clock signal is input; and

a second integrating circuit interposed between the second current source circuit for the slave circuit and the terminal to which a complementary clock signal is input.

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5. (withdrawn): The static flip-flop circuit according to Claim 4, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second integrating circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

6. (withdrawn): A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of transistors of a size smaller than the transistors constituting the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair;

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of transistors of a size smaller than the transistors constituting the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair;

a first low-pass filter circuit interposed between the first current source circuit for the master circuit and the terminal to which a clock signal is input; and

a second low-pass filter circuit interposed between the second current source circuit for the slave circuit and the terminal to which a complementary clock signal is input.

7. (withdrawn): The static flip-flop circuit according to Claim 6, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second low-pass filter circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

8. (withdrawn): A static flip-flop circuit characterized in that it comprises:

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a master circuit including a first data reading differential pair, a first data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the first data reading differential pair, and connected to each other in parallel via a first low-pass filter circuit, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair; and

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the second data reading differential pair, and connected to each other in parallel via a second low-pass filter circuit, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair.

9. (withdrawn): The static flip-flop circuit according to Claim 8, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second low-pass filter circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

10 (withdrawn): A static flip-flop circuit characterized in that it comprises:

a master circuit including a first data reading differential pair, a first data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the first data reading differential pair, and connected to each other in parallel via a first circuit including inductance, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair; and

a slave circuit including a second data reading differential pair, a second data-hold differential pair composed of two differential pairs, having transistors of a size smaller than the transistors constituting the second data reading differential pair, and connected to each other in parallel via a second circuit including inductance, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair.

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11. (withdrawn): The static flip-flop circuit according to Claim 10, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the first and second circuits adjust the currents through the first and second data-hold differential pairs to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs.

12. (withdrawn): The static flip-flop circuit according to any one of Claims 4, 6, 8 and 10, wherein, when the operating speed of the flip-flop circuit lowers from the maximum operating speed, the currents through the first and second data-hold differential pairs are adjusted to be equal to or lower than the permissible current level of the transistors constituting the data-hold differential pairs, depending on the operating speed.

13. (currently amended): The static flip-flop circuit according to ~~any one of Claims~~Claim 1~~, 2, 4 and~~ 6, wherein, when ~~the~~ operating speed of the flip-flop circuit lowers from the maximum operating speed, the currents through the first and second data-hold differential pairs increase, and at the minimum operating speed the current through the first data-hold differential pair becomes equal to the current through the first data reading differential pair and the current through the second data-hold differential pair becomes equal to the current through the second data reading differential pair.

14. (currently amended): The static flip-flop circuit according to ~~any one of Claims~~Claim 1~~, 2, 4 and~~ 6, wherein the sum of the current through the first data-hold differential pair and the current through the first data reading differential pair is equal to the current of the first current source circuit, and the sum of the current through the second data-hold differential pair and the current through the second data reading differential pair is equal to the current of the second current source circuit.